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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,016	08/26/2003	Martin Alter	M-085	3466

7590 07/22/2004

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,016	ALTER, MARTIN	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *2,3,6-8 and 10-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group I, species A, claims 1, 4, 5 and 9 in Paper No. 3, with partial traverse is acknowledged. The partial traversal is on the ground(s) that in the requirement for an election, Groups I and II differ only in a semiconductor device and method for making the same. Requiring an election based on the above-noted differences would appear to be unwarrant since the fields of search appear to be almost identical. This is not found persuasive because referring to the restriction requirement set forth in the Office Action paper no. 2, it clearly shows that the alternative method proposed by the examiner would be distinct from the process claimed. Additionally, the search is not coextensive as evidenced by the different fields of search for the process and product as cited in the previous restriction requirement. Furthermore, Applicant has not provided a convincing argument that the materially different processes would not be suitable in producing the claimed device.

The requirement is still deemed proper and is therefore made **FINAL.**

Information Disclosure Statement

2. The Information Disclosure Statement filed on 08-26-03 has been considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Sabin et al. (US Pat. 6734093) and Hashimoto (US Pat. 6255737).

Regarding claim 1, 4 and 5, the APA discloses an integrated circuit (IC) structure comprising:

- a circuit die (101 in Fig. 1B)
- an input-output pad (103 in Fig. 1B) for connecting to the circuit die
- wafer-level packaging (WSP) including a dielectric/resin material layer (111/113 in Fig. 1B) superjacent said die and a conductive material beam (CMB-109 in Fig. 1B) encapsulated in the dielectric/resin material layer and leading to a connector bump (107 in Fig. 1B) on an external surface of the dielectric/resin material

(Fig. 1B; Fig. 1A-2; specification pages 1-4).

The APA fails to teach at least one active circuit element such as a capacitor being integrated in the WSP with at least a segment of the conductive beam, the capacitor having a first plate formed by a predefined region of said beam and a grounded second

plate embedded in a top level metallization layer of the die proximate the predetermined region.

Sabin et al. teach forming an active circuit beneath a metallization structure including bonding pad metal layer/CMB where the active circuits includes conventional circuits such as a capacitor, resistor, etc. where such circuits provide a function of electrostatic discharge (ESD) protection (see Col. 3, line 47- Col. 4, line 7; Fig. 1-6; Col. 2-4). Furthermore, the metallization structure includes a conventional capacitor structure having the bonding pad metal layer/first plate and a metal layer/second plate separated by a dielectric layer (see 50, 20 and 30 respectively in Fig. 2; Col. 2, lines 15-65).

Hashimoto teaches a conventional metallization structure (Fig. 16/17A; Col. 14 and 15) in an IC having a plurality of metal layers/conductors separated by a dielectric/insulating layer including a first metal layer/conductor and a second metal layer/internal conductor separated by a dielectric/insulating layer (332/316 and 320 respectively in Fig. 16) where the second metal layer/internal conductor is grounded (see 316 in Fig. 16 and 17A; Col. 14, line 21) to provide a protection against signal noise/static discharge related problems (Col. 15, lines 42-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one active circuit element such as a capacitor/ESD capacitor being integrated in the WSP with at least a segment of the conductive beam, the capacitor/ESD capacitor having a first plate formed by a

predefined region of said beam and a grounded second plate embedded in a top level metallization layer of the die proximate the predetermined region as taught by Sabin et al. and Hashimoto so that the desired ESD protection and noise reduction can be achieved and the reliability/performance of the IC structure can be improved in the APA.

Regarding claim 9, APA, Sabin et al. and Hashimoto teach substantially the entire claimed structure as applied to claim 1, 4 and 5 above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

Nitin Parekh

PATENT EAMINER

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